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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,323	10/24/2003	Xiao Yang	021713-000300US	8239

20350 7590 11/29/2005

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EXAMINER	
BROWN, JAYME L	
ART UNIT	**PAPER NUMBER**
1733	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,323	YANG, XIAO	
	Examiner	Art Unit	
	Jayme L. Brown	1733	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) *31-60* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-30, drawn to a method for hermetically sealing devices, classified in class 156.

   II. Claims 31-60, drawn to a system for hermetically sealing devices, classified in class 257.

2. The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product as claimed can be made by another and materially different process, such as aligning the transparent member with a substrate that also has a standoff region to help with the alignment or wherein there are trenches in the transparent layer to catch excess sealing material.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Mr. Richard Ogawa on October 6, 2005 a provisional election was made with traverse to prosecute the invention of Group I,

claims 1-30. Affirmation of this election must be made by applicant in replying to this Office action. Claims 31-60 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 322. **Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application.** Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

6. The disclosure is objected to because of the following informalities:

On page 9, line 21, "Through holes 354" should be changed to - - Through holes 348 - -.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 8 and 20-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites the limitation "the standoff layer" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Regarding claims 20 and 21, it is unclear what is considered the first and second surface regions. Paragraph [0047] refers to a lower surface of the standoff region that has a surface roughness. Is that considered the first surface region? Is the second surface region the top of the recessed region?

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-4, 9-10, 18-19, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bergstedt et al. (WO 01/29890) in view of the Admitted Prior Art or Degani et al. (U.S. Patent 6,396,711)

Regarding claim 1, Bergstedt et al. teaches a method for hermetically sealing devices, the method comprising: providing a substrate, the substrate including a plurality of devices, each being arranged in a spatial manner as a first array, the array configuration including a plurality of first street regions arranged in strips and a plurality of second street regions intersecting the first street regions to form the array configuration; providing a glass member of predetermined thickness, the glass member including a plurality of recessed regions within the predetermined thickness and arranged in a spatial manner as a second array, each of the recessed regions being bordered by a standoff region, the standoff region having a thickness defined by a portion of the predetermined thickness; aligning the transparent member in a manner to couple each of the plurality of recessed regions to a respective one of said plurality of devices whereupon the standoff region being coupled to each of the plurality of first street regions and being coupled to each of the plurality of second street regions to enclose each of the devices within one of the respective recessed regions; and hermetically sealing each of the devices within one of the respective recessed regions by contacting the standoff region of the transparent member to the plurality of first street regions and second street regions using at least a bonding process to isolate each of the devices within one of the recessed regions (Page 4, line 28 – Page 6, line 1; Figures 2a, 2b, and 3).

Bergstedt et al. is silent toward the glass member being transparent and that the devices are chips that include a plurality of devices. The Admitted Prior Art teaches that it is known to use MEMS chips (array of micro-mirrors) and a transparent substrate,

because in applications, such as optical reflection off an array of micro-mirrors, a transparent member allows the top of the silicon integrated circuit to be illuminated with optical energy that is reflected with high efficiency.

Degani et al. also teaches using MEMS devices (chips with devices) and having a transparent windowpane. The windowpane is transparent to the desired wavelength used for the optical beams being deflected in the MEMS devices (Column 4, lines 6-10; Figure 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a transparent member and a plurality of chips (MEMS) in the method of Bergstedt et al. since it is conventional practice in an application that requires reflecting optical energy, as exemplified by the Admitted Prior Art and Degani et al.

Regarding claim 2, one skilled in the art would have readily appreciated choosing dimensions of the streets that are appropriate for the application and accommodate objects such as standoff regions and bonding pads. It would have been obvious to one or ordinary skill in the art at the time the invention was made to choose dimensions of the streets, such as widths in the range of about 0.5 mm to 1.0 mm, to accommodate the application in the method of Bergstedt et al. as modified above.

Regarding claim 3, one skilled in the art would have readily appreciated the transparent member having an optical power transmittance or greater than about 99%, since it is necessary to have a transparent member with excellent optical qualities when the application requires reflecting optical energy and because it is desired to have optical energy illuminate the top of the silicon integrated circuit (reach the array of

micro-mirrors). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a transparent member with an optical power transmittance or greater than about 99% in the method of Bergstedt et al. as modified above.

Regarding claim 4, Bergstedt et al. is silent toward the coefficient of thermal expansion of the transparent member being about the same as the coefficient of thermal expansion of the substrate. Degani et al. teaches that one would want uniform thermomechanical properties for the MEMS assembly (Column 4, lines 4-5). One skilled in the art would have readily appreciated having the transparent member and the substrate with similar coefficients of thermal expansion, since they will expand and react to heat in a similar manner and stay sealed. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the transparent member and the substrate with similar coefficients of thermal expansion in the method of Bergstadt et al., as modified above, as suggested by Degani et al.

Regarding claim 9, Bergstadt et al. teaches that the bonding process is selected from at least a plasma activated bonding, eutectic bonding, glue layer or adhesive bonding, welding, anodic bonding, and fusion bonding (Abstract).

Regarding claim 10, one skilled in the art would have readily appreciated having a transparent member characterized by a thickness that accommodates that chips (devices) that it is covering. It would have been obvious to one of ordinary skill in the art at the time the invention was to choose thickness, such as from about 0.1 mm to 1.2

mm, that accommodates the application and the chips (devices) that are used in it in the method of Bergstadt et al. as modified above.

Regarding claims 18 and 19, Bergstadt et al. teaches that the substrate is a silicon wafer (Page 5, line 19).

Regarding claim 23, one skilled in the art would have readily appreciated choosing a depth for the recessed region that would accommodate the chips that it would be covering. It would have been obvious to one of ordinary skill in the art at the time the invention was made to choose a depth, such as about 0.5 mm and less, that would work for the application and accommodate the chips in the method of Bergstadt et al. as modified above.

11. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bergstedt et al. (WO 01/29890) in view of the Admitted Prior Art or Degani et al. (U.S. Patent 6,396,711) as applied to claims 1-4, 9-10, 18-19, and 23 above, and further in view of Lytle et al. (U.S. Pub. 2004/0087053).

Regarding claims 11-13, Bergstedt et al., the Admitted Prior Art, and Degani et al. are relied upon for the teachings above. Bergstedt et al. is silent toward the chips being maintained in an inert environment. Lytle et al. discloses a method for encapsulating micromechanical elements or features on a substrate. Lytle et al. teaches that it is known that when hermetically sealing the capped wafer structure to the semiconductor substrate wafer in a controlled environment that comprises inert gas, the inert gas, such as helium, argon, or nitrogen, is captured in the cavity. This controlled

environment provides a predetermined damping action for mechanical motion of the device (Abstract; Page 1, paragraph [0010]; Figure 1).

One skilled in the art would have readily appreciated having the ships maintained in an inert environment as it is a conventional practice when encapsulating micromechanical elements or features on a substrate. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the chips in an inert environment in the method of Bergstedt et al., as modified above, as suggested by Lytle et al.

Regarding claim 14, one skilled in the art would have readily appreciated that the inert environment would cause a reduction in electrical breakdown, because there wouldn't be moisture in the environment that could cause electrical breakdown. It would have been obvious to one of ordinary skill in the art at the time the invention was made that the inert environment of Lytle et al. would cause a reduction in electrical breakdown in the method of Bergstedt et al., as modified above.

12. Claims 5 and 24-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bergstedt et al. (WO 01/29890) in view of the Admitted Prior Art or Degani et al. (U.S. Patent 6,396,711) as applied to claims 1, 6, 15-17, 22, and 30 above, and further in view of Cunningham et al. (U.S. Pub. 2002/0181838).

Regarding claim 5, Bergstedt et al., the Admitted Prior Art, and Degani et al. are relied upon for the teachings above. Bergstedt et al. is silent toward the transparent

member comprising an antireflective coating disposed overlying surface regions of each of the recessed regions.

Cunningham et al. is directed to an optical MEMS device and a package including an optical through path for light to pass through. Cunningham et al. teaches applying antireflective coatings on the surfaces of the lids (recessed regions). One skilled in the art would have readily appreciated that applying an antireflective coating would reduce the internal and external reflections (increase optical efficiency), and the particular antireflective coating would depend on the wavelength of light desired to pass (Abstract; Pages 3-4, paragraph [0039]; Page 4, paragraphs [0040] and [0041]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply an antireflective coating to the recessed regions in the method of Bergstedt et al., as modified above, as suggested by Cunningham et al.

Regarding claims 24-26, Bergstedt et al., Cunningham et al., the Admitted Prior Art, and Degani et al. are relied upon for the teachings above. Bergstedt et al. is silent toward the transparent member comprising a first side and a second side, the first side being parallel to the second side, and the first side and the second side being coated with an antireflective material. Bergstedt et al. is also silent toward the coating of antireflective material reducing the reflectance of visible light at the first side and the second side to less than 2% per side, and the antireflecting material comprising MgF_2.

Cunningham et al. teaches that a light-transmissive layer (glass, silicon, or other material) (408) is coated on both sides (414) with an antireflective material. If the lid (transparent member) is made of glass, MgF_2 is a possible candidate for an

antireflective coating material (Abstract; Pages 3-4, paragraph [0039]; Page 4, paragraphs [0040] and [0041]; Figure 4). One skilled in the art would have readily appreciated that applying an antireflective coating would reduce the internal and external reflections (increase optical efficiency), and the particular antireflective coating would depend on the wavelength of light desired to pass (less than 2% reflectance of visible light). One skilled in the art would also have readily recognized that MgF_2 is a conventional antireflective material. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply an antireflective coating to both sides of the transparent member and to choose a material (such as MgF_2) that would let the desired wavelength of light to pass in the method of Bergstedt et al., as modified above, as suggested by Cunningham et al.

Regarding claims 28 and 29, Bergstedt et al., the Admitted Prior Art, and Degani et al. are relied upon for the teachings above. Bergstedt et al. is silent toward each of the recessed regions having a peripheral region that filters out light or a peripheral region that forms an aperture region overlying a portion of on of the respective chips.

Cunningham et al. teaches that light transmissive lids are made of glass, silicon, or other materials, depending on the frequencies of light desired to be passed (filters the wavelengths of light). Cunningham et al. also teaches that the light transmissive lid could also have an optical aperture (114) (Page 3, paragraphs [0031], [0033], and [0035]; Figures 2A-2D and 3A-3C). One skilled in the art would have readily appreciated having one of these peripheral regions to control what wavelengths of light are passing through, so that they are appropriate for the MEMS device application. It

would have been obvious to one of ordinary skill in the art at the time the invention was made to have each of the recessed regions with a peripheral region that filters out light or a peripheral region that forms an aperture region overlying a portion of on of the respective chips in the method of Bergstedt et al., as modified above, as suggested by Cunningham et al.

13. Claims 1, 6, 15-17, 22, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Syllaios et al. (U.S. Pub. 2004/0219764) in view of the Admitted Prior Art or Degani et al. (U.S. Patent 6,396,711).

Regarding claim 1, Syllaios et al. teaches a method for hermetically sealing devices, the method comprising: providing a substrate, the substrate including a plurality of individual chips, each of the chips including a plurality of devices, each of the chips being arranged in a spatial manner as a first array, the array configuration including a plurality of first street regions arranged in strips and a plurality of second street regions intersecting the first street regions to form the array configuration; providing a lid member of predetermined thickness, the lid member including a plurality of recessed regions within the predetermined thickness and arranged in a spatial manner as a second array, each of the recessed regions being bordered by a standoff region, the standoff region having a thickness defined by a portion of the predetermined thickness; aligning the transparent member in a manner to couple each of the plurality of recessed regions to a respective one of said plurality of chips whereupon the standoff region being coupled to each of the plurality of first street regions and being coupled to

each of the plurality of second street regions to enclose each of the chips within one of the respective recessed regions; and hermetically sealing each of the chips within one of the respective recessed regions by contacting the standoff region of the transparent member to the plurality of first street regions and second street regions using at least a bonding process to isolate each of the chips within one of the recessed regions (Page 1, paragraph [0004]; Pages 1-2, paragraph [0015]; Page 2-3, paragraphs [0016], [0018], and [0021]; Figures 1, 3, and 7).

Syllaios et al. teaches that the lid member can be made of a silicon wafer, but any other suitable substrate material may be used (Page 2, paragraph [0021]). Syllaios is silent towards the lid member being transparent. The Admitted Prior Art teaches that it is known to use MEMS chips (array of micro-mirrors) and a transparent glass substrate, because in applications, such as optical reflection off an array of micro-mirrors, a transparent member allows the top of the silicon integrated circuit to be illuminated with optical energy that is reflected with high efficiency.

Degani et al. also teaches using MEMS devices (chips with devices) and having a transparent windowpane. The windowpane is transparent to the desired wavelength used for the optical beams being deflected in the MEMS devices (Column 4, lines 6-10; Figure 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a transparent member in the method of Syllaios et al. since it is conventional practice in an application that requires reflecting optical energy, as exemplified by the Admitted Prior Art and Degani et al.

Regarding claim 6, Syllaios et al. teaches that the recessed regions are formed by a process selected from dry or wet etching, laser machining, acoustic machining, and casting (Page 2, paragraph [0021]).

Regarding claim 7, Syllaios et al. teaches that the lid member comprises a first transparent member (as modified above in claim 1) overlying a standoff layer, the standoff layer including the standoff region (Figure 3).

Regarding claims 15-17, Syllaios teaches that each of the chips comprise an interconnect region that is outside of the recessed region. The interconnect region is exposed through a through hole region on the transparent member that is made when the lid wafer is opened by dicing, etching, etc. to expose the bonding pads. Also, the interconnect region comprises a plurality of bonding pads (Pages 2-3, paragraphs [0018] and [0021]; Figure 1).

Regarding claim 22, Syllaios et al. shows a recessed region (34) in a semi-annular shape (Figure 7). One skilled in the art would have readily appreciated the recessed region being different shapes, such as an annular shape, to accommodate the chips for the application. It would have been obvious to one of ordinary skill in the art at the time the invention was made to choose a shape that accommodates the application and the chips being covered in the method of Syllaios et al. as modified above.

Regarding claim 30, Syllaios et al. teaches that at least one of the plurality of devices comprises a plurality of charge coupled devices, a plurality of deflection devices, a plurality of sensing devices, and an integrated circuit device (Page 1, paragraphs [0003] and [0005]).

15. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Syllaios et al. (U.S. Pub. 2004/0219764) in view of the Admitted Prior Art or Degani et al. (U.S. Patent 6,396,711) as applied to claims 1, 6, 15-17, 22, and 30 above, and further in view of Beyne et al. (U.S. Patent 6,566,745).

Regarding claim 27, Syllaios et al., the Admitted Prior Art, and Degani et al. are relied upon for the teachings above. Syllaios et al. also teaches that after the lid wafer and device wafer are bonded the result is a plurality of individually-packaged MEMS devices that can be separated into individual devices by dicing or sawing through the wafer assembly between the devices (portions of the street regions). Sylliaos et al. is silent toward the additional steps of attaching chips to a lead frame structure, wiring bonding chips to the lead frame structure, and encapsulating the wire bond while maintaining a surface region of the transparent substrate defined on the recessed region free of encapsulant.

Beyne et al. is directed an image sensor packaging technique where a transparent cover is attached to a semiconductor substrate obtaining a hermetic seal. The obtained structure can be connected through wire bonding. Beyne et al. teaches dicing the wafer into individual chips (devices), attaching the imaging device to the BGA substrate (lead frame), wiring bonding the chips to the BGA substrate (lead frame), and encapsulating the wire bond with epoxy (Abstract; Column 12, lines 9-25; Figures 11D-11H). One skilled in the art would have readily appreciated performing these steps to complete the package as they are conventional steps and materials worked upon in the art. It would have been obvious to one of ordinary skill in the art at the time the

invention was made to perform the above steps to complete the packaging of the individual chips (devices) in the method of Sylliaos et al., as modified above, as suggested by Beyne et al.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Jayme L. Brown** whose telephone number is **571-272-8386**. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Crispino can be reached on 571-272-1226. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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